

Low Power LCD Driving Scheme

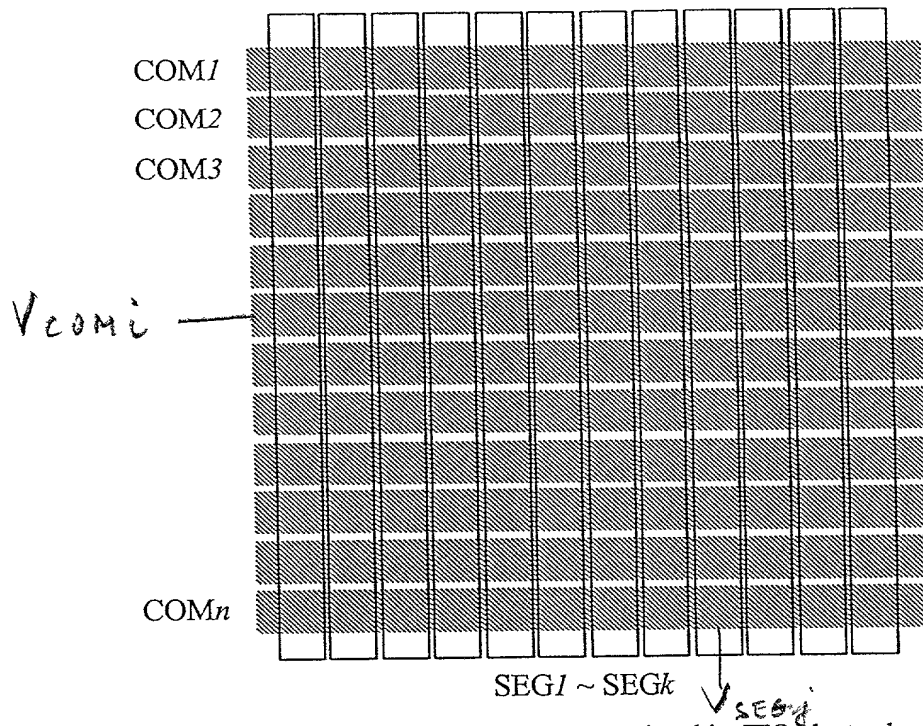


Fig. 1 A see through view of a LCD panel and its ITO electrodes

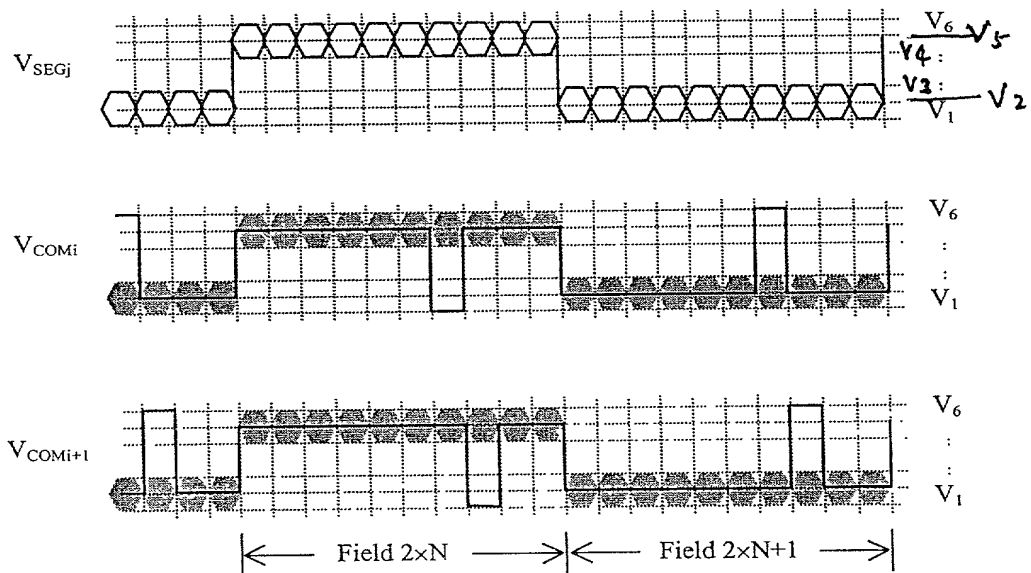


Fig. 2a IAPT driving Wave forms for COM electrodes and SEG electrodes

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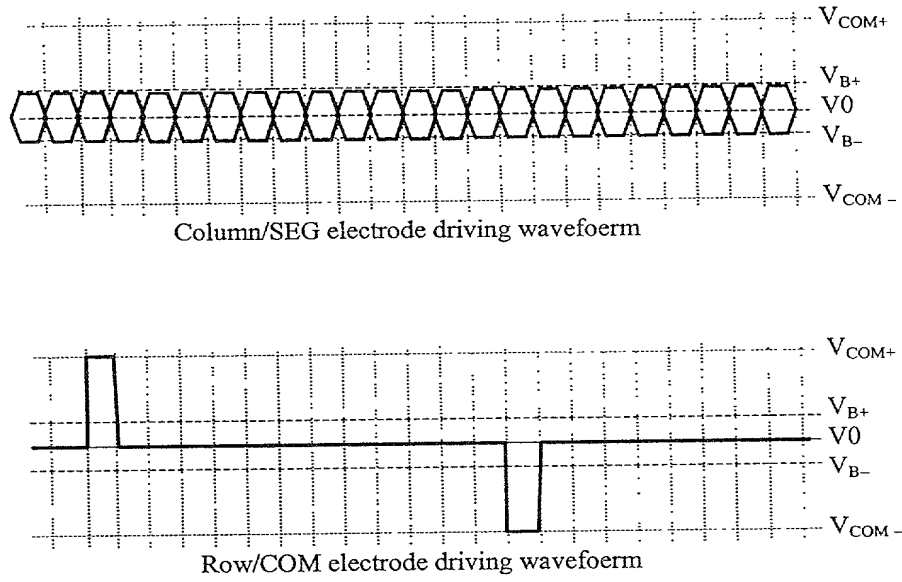


Fig. 2b APT driving Wave forms for COM electrodes and SEG electrodes

FIG. 3a is a schematic diagram of a circuit for a differential amplifier. The circuit includes a differential pair of transistors (not shown) with sources connected to a common source node. This node is connected to a tail current source (I_{SS}) and a tail resistor (R_{SS}). The gates of the transistors are connected to a common gate node, which is connected to a gate voltage (V_G) and a gate resistor (R_G). The drains of the transistors are connected to a common drain node, which is connected to a drain voltage (V_D) and a drain resistor (R_D). The circuit also includes a differential pair of load resistors (R_{L1}, R_{L2}) connected to the drains of the transistors. The output of the differential amplifier is taken from the drains of the transistors.

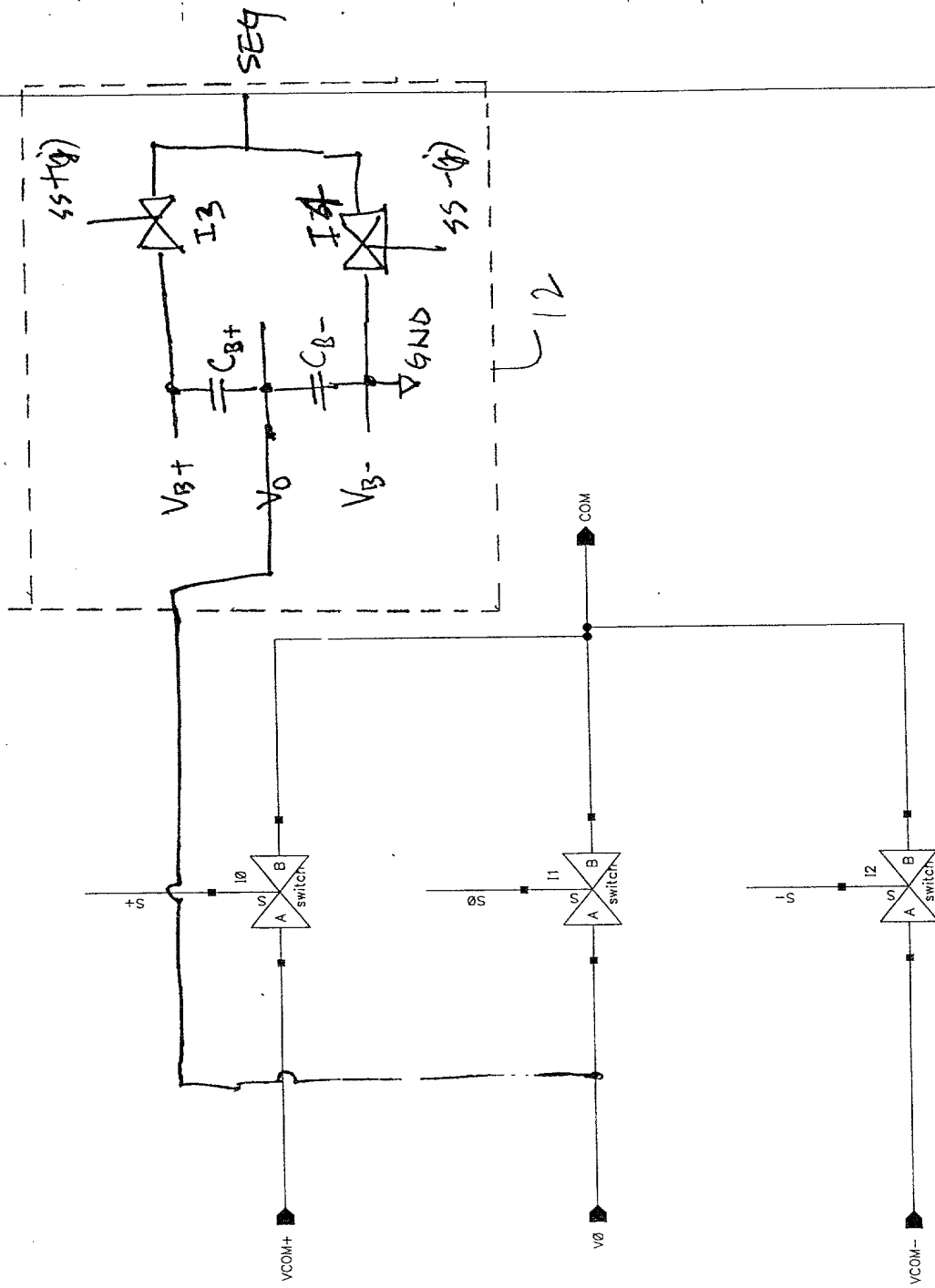


Fig. 3a

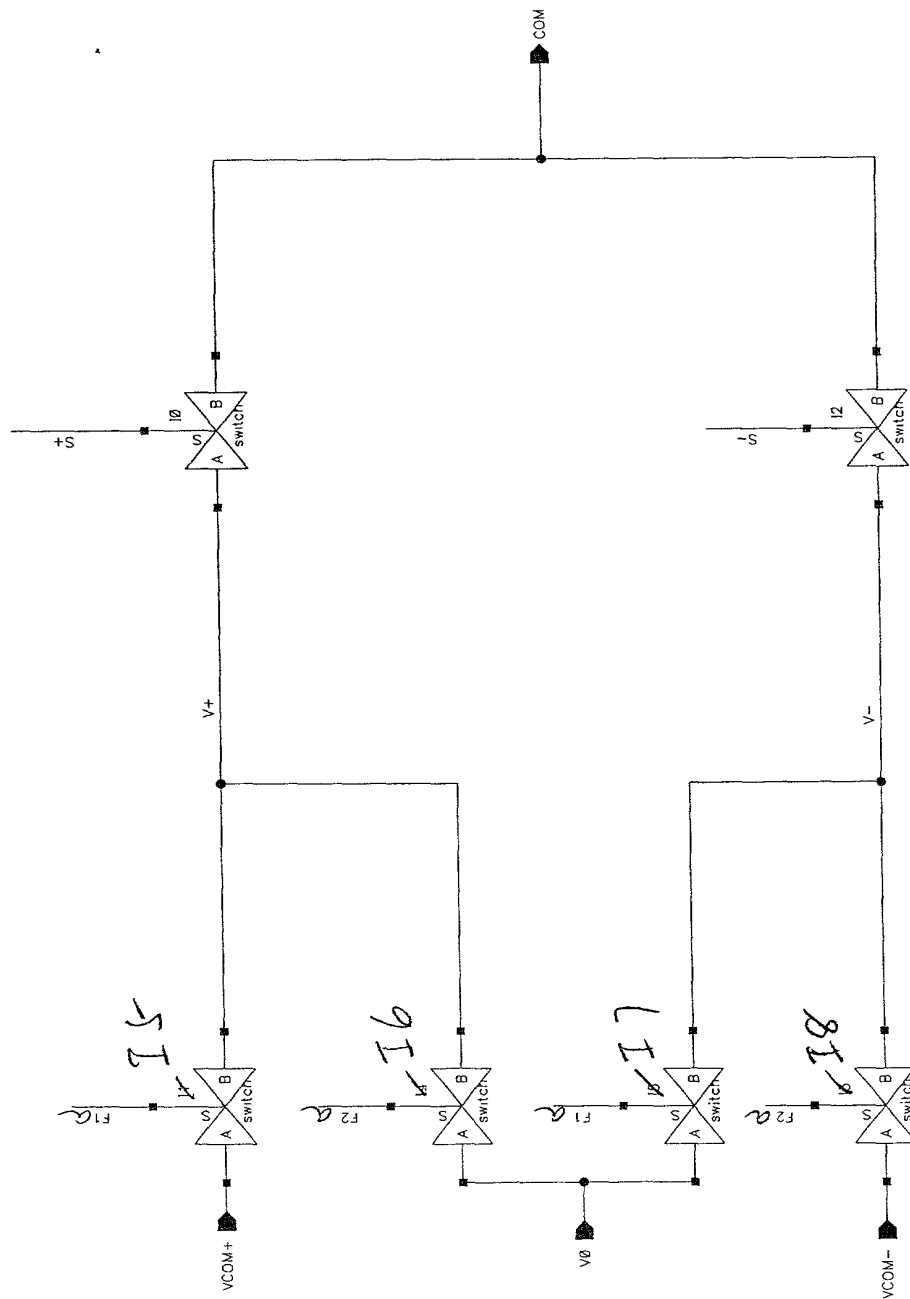


Fig. 3b

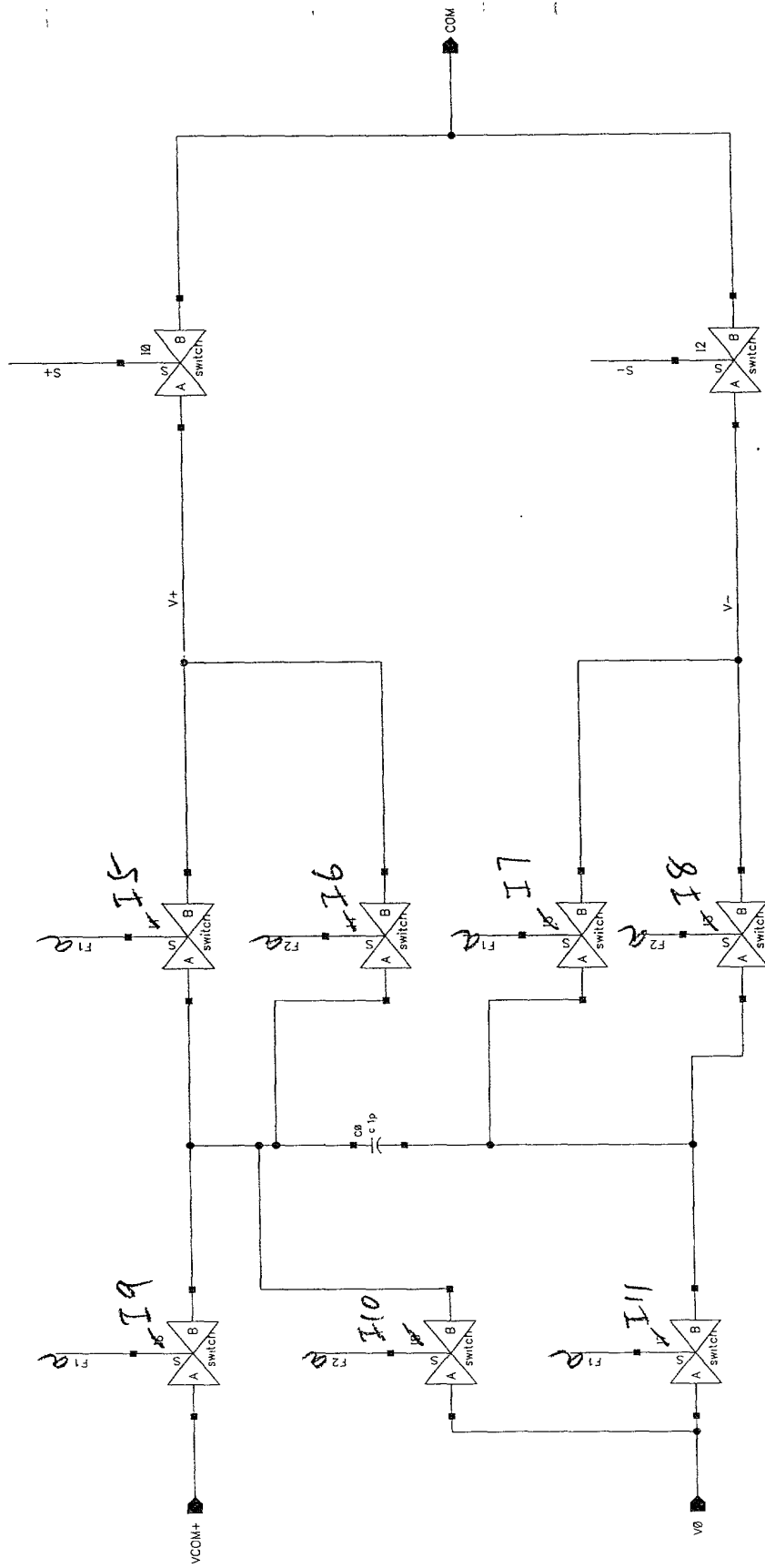


Fig. 3c

1. The circuit is a differential amplifier with a common-mode feedback (CMFB) loop. The input stage consists of two NMOS transistors (I1, I2) and two PMOS transistors (I3, I4). The gates of I1 and I2 are connected to a common-mode feedback network (I5, I6, I7, I8) which is biased by a current source (I9). The gates of I3 and I4 are connected to a common-mode feedback network (I10, I11, I12, I13) which is biased by a current source (I14). The output stage consists of two NMOS transistors (I15, I16) and two PMOS transistors (I17, I18). The gates of I15 and I16 are connected to a common-mode feedback network (I19, I20, I21, I22) which is biased by a current source (I23). The gates of I17 and I18 are connected to a common-mode feedback network (I24, I25, I26, I27) which is biased by a current source (I28). The output of the amplifier is taken from the drains of I15 and I16.

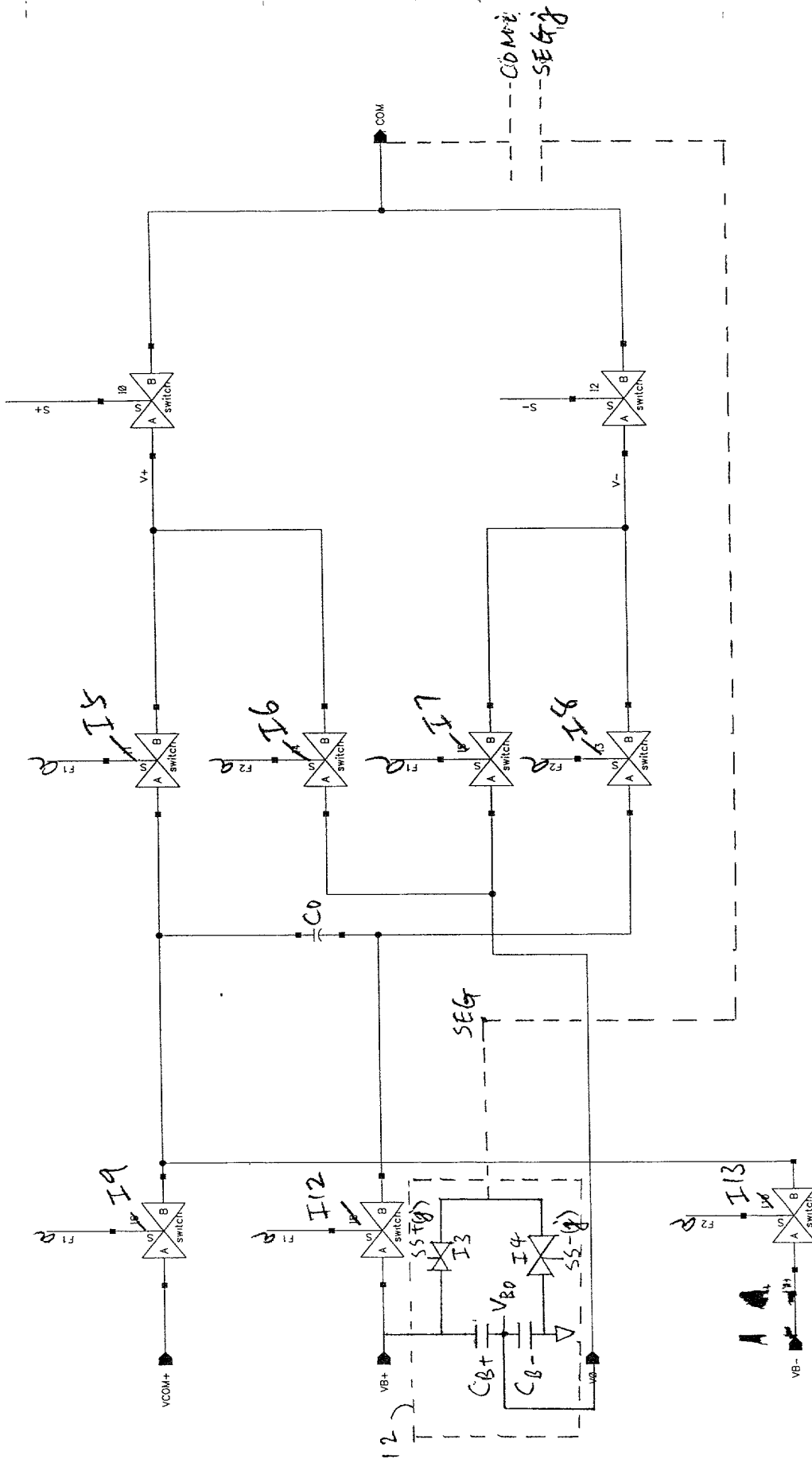
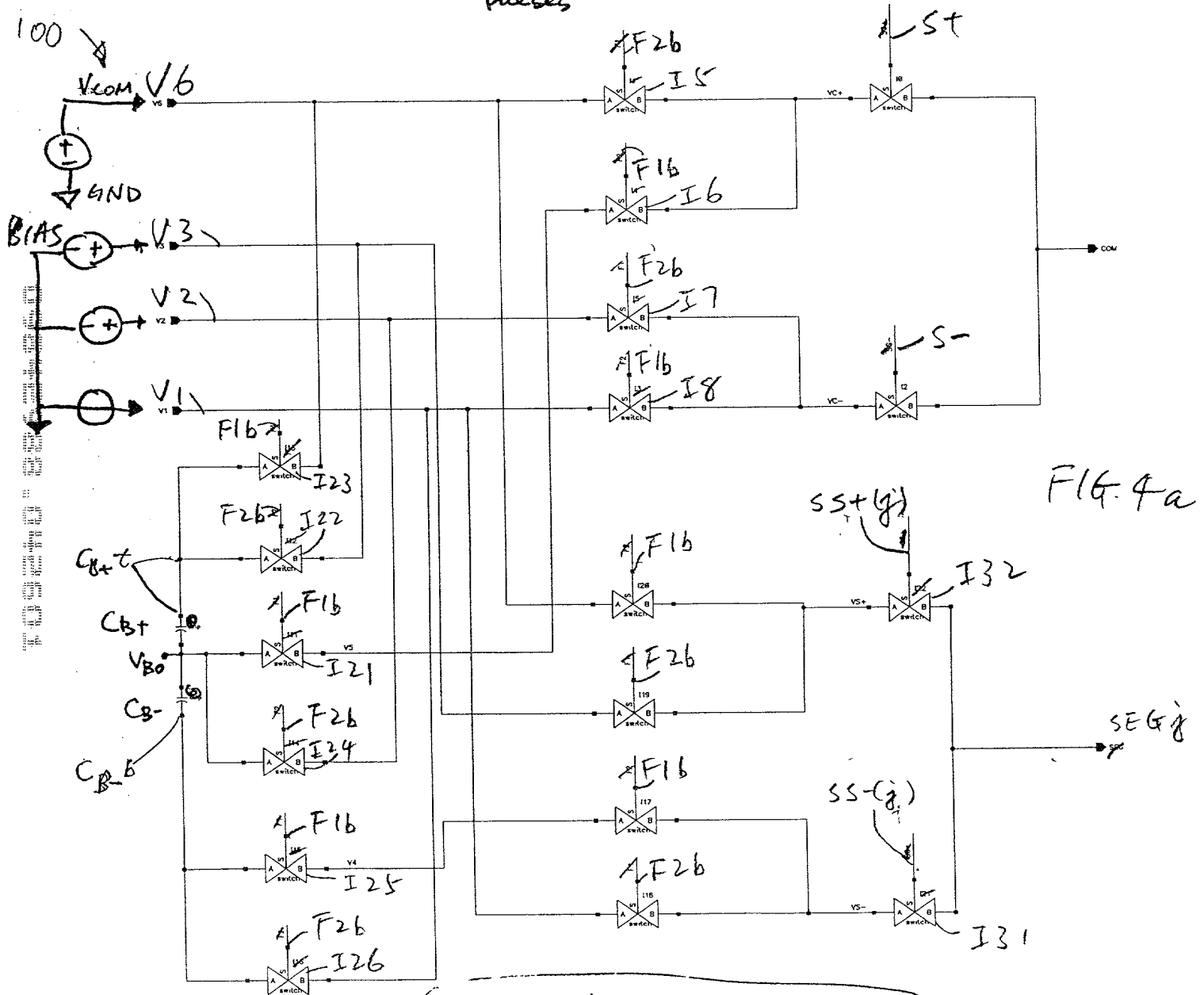
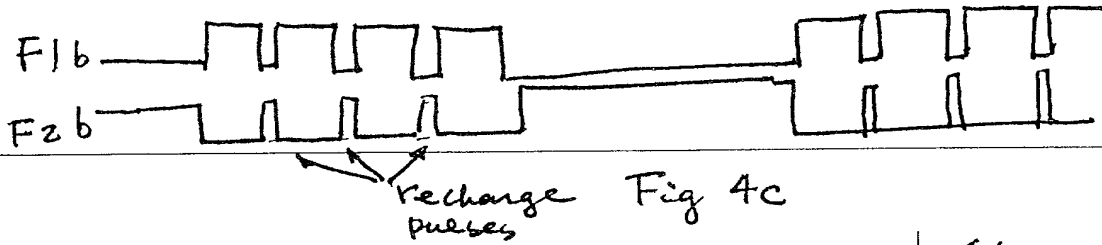
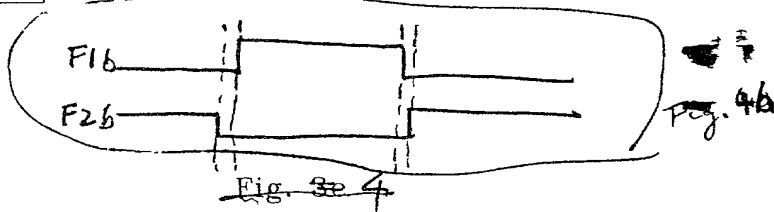
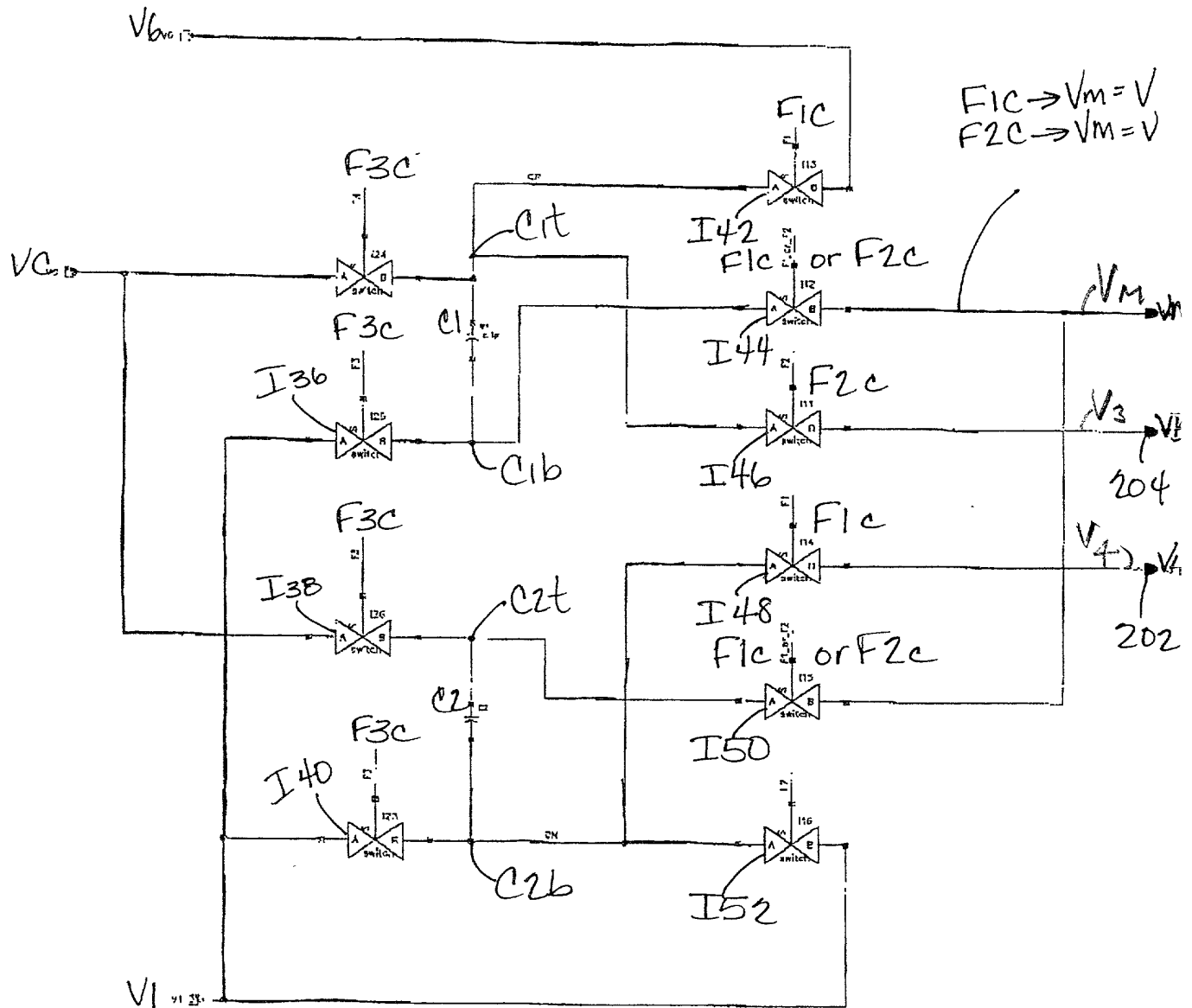


Fig. 3d



$$F2b = \overline{F1b}$$





200a

Fig. 315a

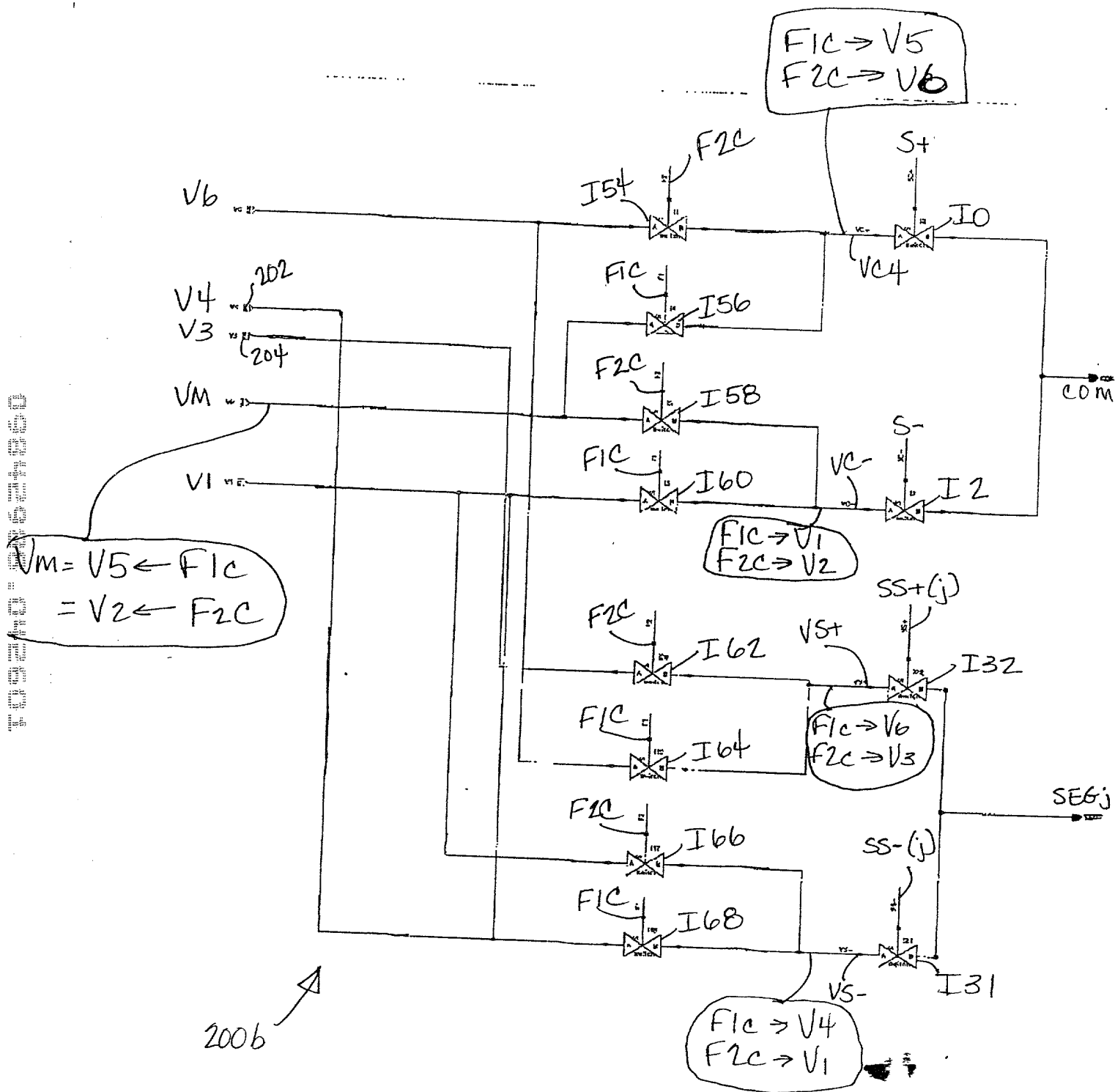


Fig. 35b

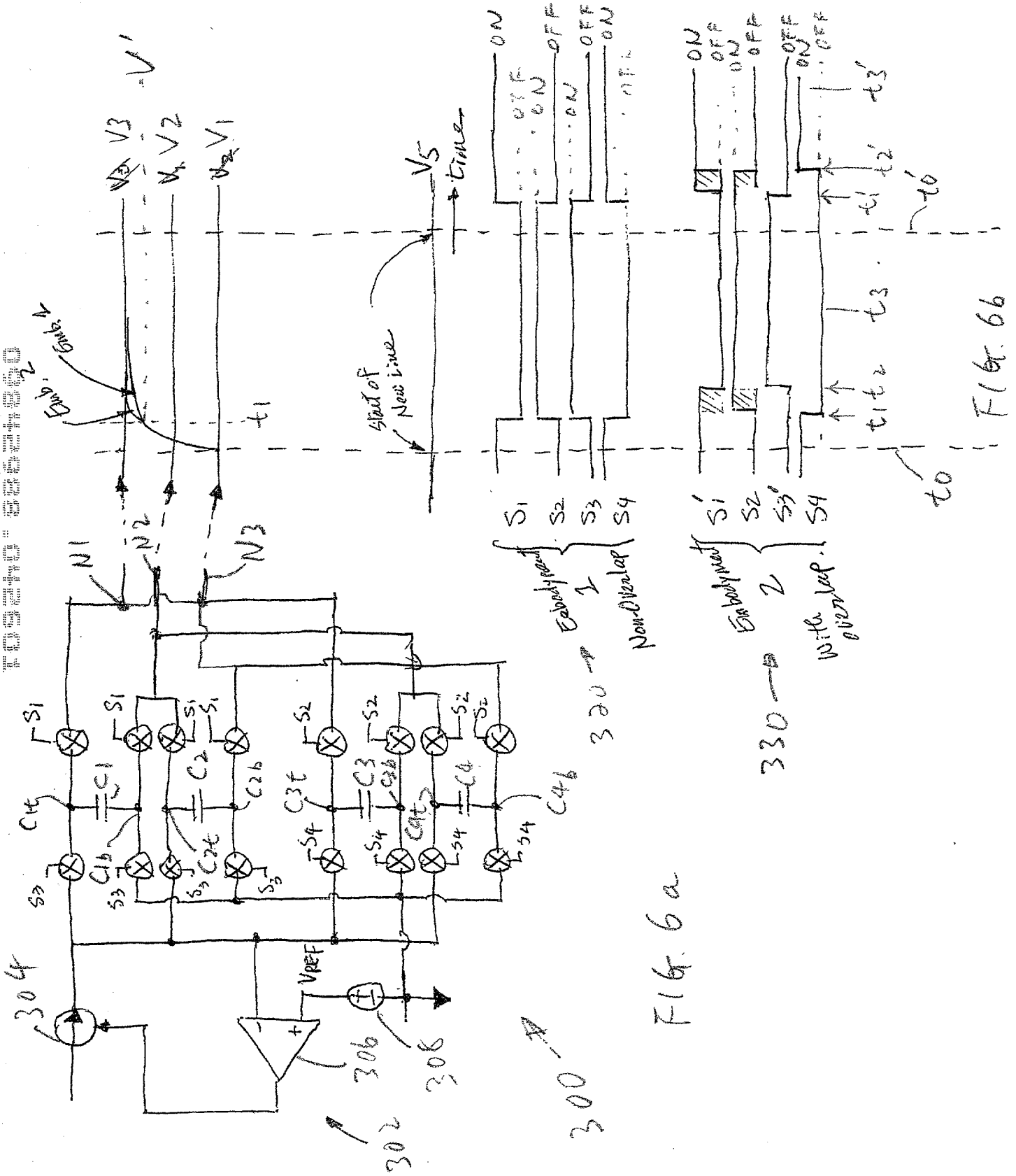


FIG. 6a

FIG. 6b